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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/587,608	07/27/2006	Francesco Pessolano	NL04 0078 US1	9958

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EXAMINER	
PATHAK, SUDHANSHU C	
ART UNIT	PAPER NUMBER
2611	

NOTIFICATION DATE	DELIVERY MODE
08/05/2010	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ip.department.us@nxp.com

Office Action Summary	Application No.	Applicant(s)	
	10/587,608	PESSOLANO, FRANCESCO	
	Examiner	Art Unit	
	SUDHANSHU C. PATHAK	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 February 2010*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-18 are pending in the application.

Response to Arguments

2. Applicant's arguments, filed in amendment dated 02/23/2010, with respect to claims 1-18 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-9, 13-14, 16-17 (device) & 15, 18 (method) are rejected under 35 U.S.C. 103(a) as being unpatentable over Liu et al. (6,219,797) in view of Cheng (2002/0172309).

In regards to Claims 1-2, 9, 14-18, Liu discloses an electronic device (method) for generating a clock signal for an integrated circuit (Fig. 5), the device comprising: at least two clock generation elements configured to generate a single clock signal at a clock output in response to an input signal and to operate in a mutually exclusive manner, the outputs of said clock generation elements being selectively connectable to said clock output the device (Fig. 5, element 74, 86, 78) {Interpretation: The reference discloses the division elements generating multiple

clocks and further the "Mux" selects a single clock from the multiple options}: means for receiving a data pattern representative of a sequence of frequencies at which said clock signal is required to be generated (Fig. 5, elements "CD0" & "CD1") {Interpretation: The reference discloses a plurality of bits (patterns) so as to select different frequency signals and the selection of a certain bit (pattern) selects a certain frequency clock. This interpretation is consistent with the instant application specification as recited on Page 5, lines 28-29 which states "The device comprises an arbiter 22 for receiving requests to change the frequency of the clock signal...", thus each bit combination of "CD0" & "CD1" is interpreted as a request. Furthermore, the claim does not recite receiving a single pattern representing all the plurality of frequencies}; means for causing a clock generation element other than the clock generation element generating the clock signal at the immediately previous frequency in said sequence to generate a clock signal at said next frequency and means for causing the clock signal at the immediately previous frequency in said sequence to be disconnected from said clock output and further means for causing the clock signal at the next frequency in said sequence to be connected to said clock output (Fig. 5, element 74, 78, 86) {Interpretation the reference discloses plurality of different clock generation elements i.e. div. "1024", "64" wherein the clock generation elements are different and depending on the pattern the other elements are disconnected or connected depending on the desired clock frequency}; wherein the clock generation element being caused to generate a clock signal at each frequency in said sequence is independent of the value of said frequency (Fig. 5, element 70,

72, 74, 78, 86 & Column 12, lines 53-67) {Interpretation: The reference discloses plurality of clock source elements i.e. crystal and ring oscillator which are separate and independent and the clock generation elements can generate frequencies with either source}. However, Liu does not disclose the data pattern representative of a sequence of two or more frequencies at which the clock signal is required to be generated.

Cheng discloses the data pattern representative of a sequence of two or more frequencies at which said clock signal is required to be generated by a PLL circuits (Paragraphs 5, 23). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention that Cheng teaches a data pattern representative of a sequence of two or more frequencies at which said clock signal is required to be generated and this is implemented in the device as described in Liu so as to be able to vary the frequency of the clocks in the system in a predetermined manner and time.

In regards to Claim 3, Liu in view of Cheng discloses an electronic device for generating a clock signal for an integrated circuit as described above. Liu further discloses generation of the clock signal at said next frequency in said sequence is commenced prior to disconnection of the clock signal at the immediately previous frequency in the sequence from the clock output (Column 14, lines 54-60 & Column 19, lines 60-67). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention that Liu in view of Cheng satisfies the limitation of the claim.

In regards to Claims 4-8, 13, Liu in view of Cheng discloses an electronic device for generating a clock signal for an integrated circuit as described above. However, Liu in view of Cheng does not explicitly disclose wherein (dis)connection of the clock signal at the next frequency in said sequence to said clock output is caused to occur when said clock signal is low. However, it would have been obvious to one of ordinary skill in the art at the time of the invention that there is no criticality in performing the (dis)connection to the another frequency clock signal when said clock signal is low this is a matter of design choice depending on seamless (without) jitter from one clock signal to another. Furthermore, it would have been obvious to one of ordinary skill in the art at the time of the invention that there is no criticality in implementing the clock generation elements as programmable ring oscillators this is a matter of design choice so as to generate an accurate programmable clock signals so as to perform signal frequency changing based on the user. Furthermore, it would have been obvious to one of ordinary skill in the art at the time of the invention that a ring oscillator includes variable delay elements to vary the frequency of the output signal. Furthermore, it would have been obvious to one of ordinary skill in the art at the time of the invention that a controller is implemented so as to select between the clocks.

5. Claims 10-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Liu et al. (6,219,797) in view of Cheng (2002/0172309) and further in view of Applicant Admitted Prior Art (AAPA).

In regards to Claims 10-12, Liu in view of Cheng discloses an electronic device for generating a clock signal for an integrated circuit as described above. However, Liu in view of Cheng does not explicitly disclose an arbiter for determining the order in which said requests are to be affected wherein further said arbiter orders said requests for action on a first-in-first-out basis.

The AAPA discloses a method for generating a clock signal from multiple clock sources (Specification, Page 4, lines 20-33) comprising an arbiter for determining the order in which said requests are to be affected wherein further said arbiter orders said requests for action on a first-in-first-out basis (Specification, Page 6, lines 9-15). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention that AAPA teaches an arbiter for determining the order in which said requests are to be affected wherein further said arbiter orders said requests for action on a first-in-first-out basis and this is implemented in the method as described in Liu in view of Cheng so as to implement multiple requests for change in frequency of clock simultaneously. Furthermore, it would have been obvious to one of ordinary skill in the art at the time of the invention that there is no criticality in selecting requests that are received at substantially the same time, the arbiter is arranged to randomly select the order in which action is taken on these two requests this is a matter of design choice so as to be able to avoid losing any of the requests.

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to SUDHANSHU C. PATHAK whose telephone number is (571)272-5509. The examiner can normally be reached on 9am-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chieh M. Fan can be reached on 571-272-3042.

The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Sudhanshu C Pathak/
Primary Examiner, Art Unit 2611